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APPLICATION
FOR
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LETTERS PATENT

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FOR:	**SURGE PROTECTION CIRCUIT FOR SEMICONDUCTOR DEVICES**
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TITLE OF THE INVENTION

Surge Protection Circuit for Semiconductor Devices

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a surge protection circuit for semiconductor devices, particularly suitable for use in active matrix liquid crystal displays.

Description of the Related Art

Japanese Patent Publication 11-119256 discloses a surge protection circuit for a TFT (thin-film transistor) array of liquid crystal display elements connected to intersections of vertical and horizontal signal lines. The drains of all switching transistors are respectively connected to the vertical signal lines and the gates of all switching transistors are respectively connected to the horizontal signal lines. The prior art surge protection circuit is composed of a first array of bi-directional nonlinear circuits associated with the vertical lines and a second array of bi-directional nonlinear circuits associated with the horizontal lines. Each protection circuit is formed by a pair of first and second thin-film transistors. In each protection circuit, the drain and gate of the first transistor are connected together to a reference voltage terminal to which the source of the second transistor is also connected, and the drain and gate of the second transistor are connected together to the associated signal line to which the source of the first transistor is also connected. The vertical and horizontal signal lines are terminated at corresponding pad terminals. When high-voltage static energy builds up on a pad terminal of the LCD array, one of the associated transistors is turned to provide a low-impedance

path for the static energy.

During manufacture of a protection transistor, an interlayer contact is established between the drain and the gate region by forming a contact hole (throughhole) in the gate insulator using a mask so that part of the gate region is exposed and depositing metal in the contact hole when the drain region is completed. Alternatively, a contact hole is formed after a gate and a drain region and a contact hole is provided therebetween. The gate and drain regions are connected through the contact hole when a transparent conductive film is deposited simultaneously with the deposition of the transparent conductive film for pixel electrodes.

Study has recently been undertaken to cut down the manufacturing cost of thin film transistor arrays by reducing masking processes. Since a masking process is used for establishing an interlayer contact between drain and gate electrodes, this cost reduction approach cannot be applied to the prior art surge protection circuit.

According to Japanese Patent Publication 6-18924, surge voltage is discharged through a path established between drain electrodes of adjacent signal lines, rather than through the gate-drain interlayer contact. This is achieved by separating signal lines at intervals of a few micrometers so that capacitive coupling is established between associated pad electrodes. When a high-voltage static surge develops, a potential difference occurs between adjacent signal lines and the surge is spark-discharged through the capacitive path and all signal lines are driven to the same potential. However, since the generation of a spark is necessary for discharging surge potentials, the protection circuit is not reliable.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a surge protection transistor that can be fabricated with a reduced number of production steps.

The stated object is obtained by the provision of a floating-gate field effect transistor which is configured to form a low impedance path for a surge potential which builds up in a semiconductor device to be protected.

According to a first aspect of the present invention, there is provided a surge protection device comprising a gate electrode embedded in an insulator, a source electrode and a drain electrode on the insulator, the source and drain electrodes respectively forming first and second capacitances with the gate electrode, and a semiconductor island on the insulator. The semiconductor island forms a channel between the source and drain electrodes and a third capacitance with the gate electrode, the third capacitance being smaller than either of the first and second capacitances, the source and drain electrodes being adapted for connection to external circuitry for establishing a low-impedance path when the external circuitry is subjected to a surge potential.

According to a second aspect, the present invention provides a surge protection circuit comprising a plurality of surge protection devices. Each of the protection devices comprises a gate electrode embedded in an insulator, a source electrode and a drain electrode on the insulator, the source and drain electrodes respectively forming first and second capacitances with the gate electrode. A semiconductor island is formed on the insulator, the island forming a channel region between the source and drain electrodes and a third

capacitance with the gate electrode, the third capacitance being smaller than either of the first and second capacitances.

The source and drain electrodes of each of the surge protection devices may be respectively connected to the drain and source electrodes of adjacent ones of the plurality of surge protection devices and further connected to pad electrodes of external circuitry for establishing connections with the adjacent surge protection devices when one of the pad electrodes is subjected to a surge potential. Alternatively, the source and drain electrodes of each of the surge protection devices may be connected in series to external circuitry for establishing a low-impedance path to ground when the external circuitry is subjected to a surge potential.

According to a third aspect, the present invention provides a surge protection circuit for a semiconductor display device. The display device includes a first plurality of pad electrodes, a plurality of vertical signal lines connected respectively to the first plurality of pad electrodes, a second plurality of pad electrodes, and a plurality of horizontal signal lines intersecting the vertical signal lines, the horizontal signal lines being connected respectively to the second plurality of pad electrodes. The surge protection circuit comprises a plurality of floating-gate field effect transistors. Each transistor includes a floating gate electrode, a source electrode and a drain electrode, the source and drain electrodes of each of the transistors being respectively connected to the drain and source electrodes of adjacent ones of the plurality of floating-gate transistors and further connected to the first plurality of pad electrodes for establishing connections with the adjacent floating-gate transistors when one of the first plurality of pad electrodes or

one of the plurality of vertical signal lines is subjected to a surge potential. Alternatively, the source and drain electrodes of each of the transistors are respectively connected to the vertical signal lines for establishing a low-impedance path to ground when one of the first plurality of pad electrodes or one of the plurality of vertical signal lines is subjected to a surge potential.

BRIEF DESCRIPTION OF THE DRAWIGNS

The present invention will be described in detail further with reference to the following drawings, in which:

Fig. 1 is a top plan view of a liquid crystal display panel of a first embodiment, incorporating surge protection circuits of the present invention;

Fig. 2 is a plan view of a surge protection transistor of the present invention;

Fig. 3 is a cross-sectional view taken along the lines 2-2 of Fig. 2;

Figs. 4 to 7 are circuit diagrams of modified arrangements of the floating-gate field effect transistors of the present invention.

DETAILED DESCRIPTION

In Fig. 1, an active matrix LCD display panel according to a first embodiment of the present invention is illustrated. The display panel comprises a first plurality of pad electrodes 10 respectively connected to vertical signal lines 11 and a second plurality of pad electrodes 12 respectively connected to horizontal signal lines 13. Switching transistors, not shown, are connected to the intersections of the vertical and horizontal signal lines. Surge protection transistors 14 are floating-gate field effect transistors whose source and drain electrodes are connected to adjacent vertical signal lines 11 in such a manner that the drain of one transistor and

the source of an adjacent transistor are connected together to the same vertical signal line. Since the drain electrodes of all switching transistors are connected to the vertical signal lines and their gate electrodes are connected to the horizontal signal lines, the vertical signal lines are also called drain bus lines and the horizontal signal lines are also called gate bus lines.

In Figs. 2 and 3, a representative surge protection transistor 14 is shown fabricated on a common glass substrate 20 on which the gate 21 of the transistor is embedded in a gate insulator 22. On the gate insulator 22 is a semiconductor island 23 of amorphous silicon. The source electrode 24 and the drain electrode 25 of the transistor are formed on the opposite sides of the island 23 so that they are separated by a channel with a length "Lch", which forms a channel capacitance "Cch" with the gate 21. Source 24 and the gate 21 overlap with each other by a length "Lgs" to form a gate-source capacitance "Cgs" and the drain 25 and the gate 21 overlap with each other by a length "Lgd" to form a gate-drain capacitance "Cgd". For a gate width Wg of 24 micrometers, the overlapping lengths Lgs and Lgd are equal to 24 micrometers and the channel length Lch is 6 micrometers. Therefore, the capacitances Cgs and Cgd are equal to each other and each of these capacitances is much greater than the channel capacitance Cch.

If a positive pulse charge builds up on the source 24 of a surge protection transistor 14, the source electrode is driven sharply to a positive potential. Since the gate electrode 21 is floated in isolation, the presence of capacitances Cgs and Cgd of equal magnitude, the positive potential at the source electrode 24 raises the gate 21 to some positive level. Because capacitances Cgs and Cgd are much greater than channel capacitance Cch,

the gate potential is raised to a point that is intermediate between the source and drain potentials. Under this condition, the gate potential is higher than the potential at the drain 25 and hence, the floating-gate transistor 14 is switched to an ON state. In a similar manner, if the source electrode 24 is negatively charged, the gate electrode 21 is driven to a negative potential that is intermediate between the source and drain potentials. Since the drain electrode 25 is driven close to the ground potential, the floating-gate transistor 14 is turned ON. Because of the symmetrical configuration of the source and drain electrodes with respect to the gate, similar events occur when positive or negative static charge builds up on the drain electrode 25.

More specifically, if capacitances Cgs and Cgd are equal to twice the value of channel capacitance Cch the gate potential is approximately 40 percent of the potential rise of the source or drain electrode. If capacitances Cgs and Cgd are equal to four times the value of channel capacitance Cch the gate potential is approximately 44 percent of the potential rise of the source or drain electrode.

Due to the floating-gate field effect transistor, the need to provide contact holes is eliminated, simplifying the production steps. In addition, the bi-directional nonlinear operating characteristic can be obtained by a single floating-gate field effect transistor 14. This is advantageous for reducing the amount of space to be required for protection circuitry and allowing the protection circuit to be used for a high resolution display device in which the interval between successive vertical signal lines (or drain bus lines) is significantly small.

When one of the vertical signal lines 11 is charged with a surge

potential, the corresponding pair of floating-gate transistors 14 are switched ON. As a result, the energy at the original point divides into two charge packets, which propagate along the array of transistors 14 in opposite directions, successively switching them into ON state with decreasing potentials to allow the charge packets to escape through the associated pad electrodes 10.

The floating-gate field effect transistors of the present invention can be arranged in a number of different ways as illustrated in Figs. 4, 5, 6 and 7.

In Fig. 4, the vertical signal lines 11 of the display panel are respectively connected to the source electrodes of floating-gate field-effect transistors 15 of the present invention and their drain electrodes are connected to a common shunt line 16, which is connected to the ground. When a surge potential builds up on one of the vertical signal lines, the corresponding surge protection transistor 15 is turned ON, allowing the charge to escape to the ground. In addition to the transistors 15, the transistor array of Fig. 1 may be provided as shown in Fig. 5. Static energy can be distributed along the transistors 14 and discharged individually to the ground by the transistors 15. The distributed discharging effect of the array of transistors 14 is effectively combined with the individual ground discharging effect of transistors 15 to protect the display from significantly high surge potentials.

Fig. 6 shows a modified arrangement of the protection circuit of Fig. 1. In this modification, floating-gate field effect transistors 17A and 17B are additionally connected to the opposite ends of the array of transistors 14. Specifically, the source-drain path of transistor 17A is connected between a

transfer pad electrode 10A and the left-most transistor of the array, and the source-drain path of transistor 17B is connected between the right-most transistor of the array and a transfer pad electrode 10B. Transfer pad electrodes 10A and 10B are connected to ground. Transistors 17A and 17B provide extra ground-discharge paths to protect the display device from high potential charges. For significantly high potential surges, the arrangement of Fig. 7 is suitable in which the transistor array of Fig. 6 is combined with the array of Fig. 4.